======================== Part 1 =========================================

1.   Knowledge of Design Principles for Modern Computers

2.   Knowledge of five stage of pipelining used in microprocessor design

3.   Knowledge of superscalar architectures

4.   knowledge of PCI bus width, bus speed, and maximum data transfer rates.

5.   Understand the meaning of the following PCI signals:

     AD,  C/BE, PAR, FRAME#, TRDY#, IRDY#, STOP#,  DEVSEL#, CLK, RST#

6.  Detailed Knowledge of PCI Bus Arbitration:

    Explain what centralized arbitration is;

    Be able to explain Basic PCI arbitration form;

    Be able to explain what fairness means for PCI arbitration;

    Four different PCI bus states can be defined based on FRAME# and IRDY#

    values. What are they? What does each state mean?

    Be able to understand PCI Bus arbitration waveforms among multiple masters.

    Understand the meaning of PCI Bus Parking.

    Understand the PCI arbitrator request/grant timing requirement (Textbook page 67).

    Understand the meaning of hidden arbitration.

7.  Understand the definition of the following latency:

    Bus access latency, arbitration latency, bus acquisition latency,

    initiator and target latency.

    What is the timing requirement to prevent master from  monopolizing the bus?

    What is Master Latency Timer (LT)?

    Explain how Master latency timer (LT) works.

    Can LT Value Be Hardwired? (Textbook Page 80).

    Yes, for a master that performs one or two data phases per wansaction, but the

    hardwired value may not exceed 16 (and it could be zero). Please refer to the

    previous sections regarding the implication if you choose to hardwire a value of

    zero.

    What is the timing requirement to prevent target from  monopolizing the bus?

8.  Be able to explain single data phase read transaction waveform;

    Be able to explain burst data phase read transaction waveform;

    Be able to explain single data phase write transaction waveform;

    Be able to explain burst data phase write transaction waveform;

    Be able to discuss performance during read transaction:

    1). back-to-back single data phase read transfers

    2). the achievable burst transfer rate during the second through the last data read phases

    Be able to discuss performance during write transaction:

    1). back-to-back single data phase write transfers

    2). the achievable burst transfer rate during the second through the last data write phases

9. Be able to draw single data phase read transaction waveform;

    Be able to draw burst data phase read transaction waveform with wait states inserted;

    Be able to draw optimized burst data phase read transaction waveform without wait states inserted;

    Be able to draw single data phase write transaction waveform;

    Be able to draw burst data phase write transaction waveform with wait states inserted;

    Be able to draw optimized burst data phase write transaction waveform without wait states inserted;

======================== Part 2 =========================================

1.   Cache   (Handout)

   2.   Memory and IO Addressing (chapter 10)

1. Reflected Wave Switching (chapter 3)
2. Fast Back-to-Back & Stepping  (chapter 11)
3. Early Transaction End (chapter 12)
4. Error Detection and Handling  (chapter 13)
5. The 64-bit PCI Extension  (chapter 15)
6. 66 MHz PCI Implementation (chapter 16)
7. Configuration Address Space (chapter 17)

Students must review all of waveforms, be able to understand and also be able to draw those waveforms included in the textbook chapters for the above topics.

Details:

1. Understand the architecture of fully associative, direct mapped and set associative cache.

Be able to design direct mapped cache and set associative cache.

1. Understand dword-aligned memory addressing and quadword-aligned memory addressing; Understand linear (sequential) mode and also cache line wrap mode addressing sequence;  Understand PCI IO addressing
2. Be able to explain what Reflected-Wave Switching is.

Understand 33MHz vs. 66 MHz PCI Timing;

1. Understand back-to-back transactions and fast back-to-back transactions.;

Understand advantages and disadvantages of address/data stepping and also understand how stepping is implemented.

1. 5.1). Understand how master initiates termination;

         Master abort on single vs. multiple-data phase transaction;

         Know the difference among fast, medium, slow and subtractive device decoding;

         Understand action taken by master in response to master abort;

5.2). Using DEVSEL# and TRDY# in conjunction with STOP#, the target can

indicate one of four different termination cases  to the initiator.

Be able to explain each of the four different cases:

I). disconnect with data transfer - disconnect A and B

II). disconnect without data transfer - disconnect 1 and 2

III). Retry

IV). Target Abort

5.3). Understand STOP# not permitted during turn-around cycle

5.4). Understand resumption of disconnected transaction is optional

5.5). Understand reasons target issues disconnect

5.6). Understand reasons target issues retry

5.7). Understand reasons target issues target abort

5.8). Understand Master's response to target abort

1. Understand data/address parity generation, checking and parity error reporting on READ/WRITE transaction; Understand the usage of SERR# signal.
2. Understand 64‐bit Data Transfers and 64‐bit Addressing
3. Understand 33MHz vs. 66 MHz PCI Timing; Understand How Components Indicate 66MHz Support.
4. Understand PCI has three Address Spaces: I/O, Memory and Configuration

PCI bus masters (including the host/PCI bridge) use PCI IO and memory transactions to access PCI IO and memory locations, respectively.

In addition, a third access type, the configuration access, is used to access a device's configuration registers.

A function's configuration registers must be initialized at startup time to configure the function to respond to memory and/or IO address ranges assigned to it by the configuration software.

======================== Part 3 =========================================

1. Understand configuration address space format
2. Understand configuration mechanism including configuration address port and configuration data port.
3. Type 0 Configuration Transaction vs. Type 1 Configuration Transaction
4. Implementation of IDSEL
5. Type 0 Configuration Transaction Read Access Waveform
6. Type 0 Configuration Transaction Write Access Waveform
7. Type 1 Configuration Transaction Read Access Waveform
8. Type 1 Configuration Transaction Write Access Waveform
9. PCI-to-PCI Bridge’s Configuration Registers vs. PCI Function’s Configuration Registers
10. Be able to explain the difference among Primary PCI Bus Number Register, Secondary PCI Bus Number Register, and Subordinate PCI Bus Number Register.
11. Understand the basic Transaction Filtering Mechanism used by the PCI-to-PCI bridge.